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Soft Error Tolerant FPGA Design

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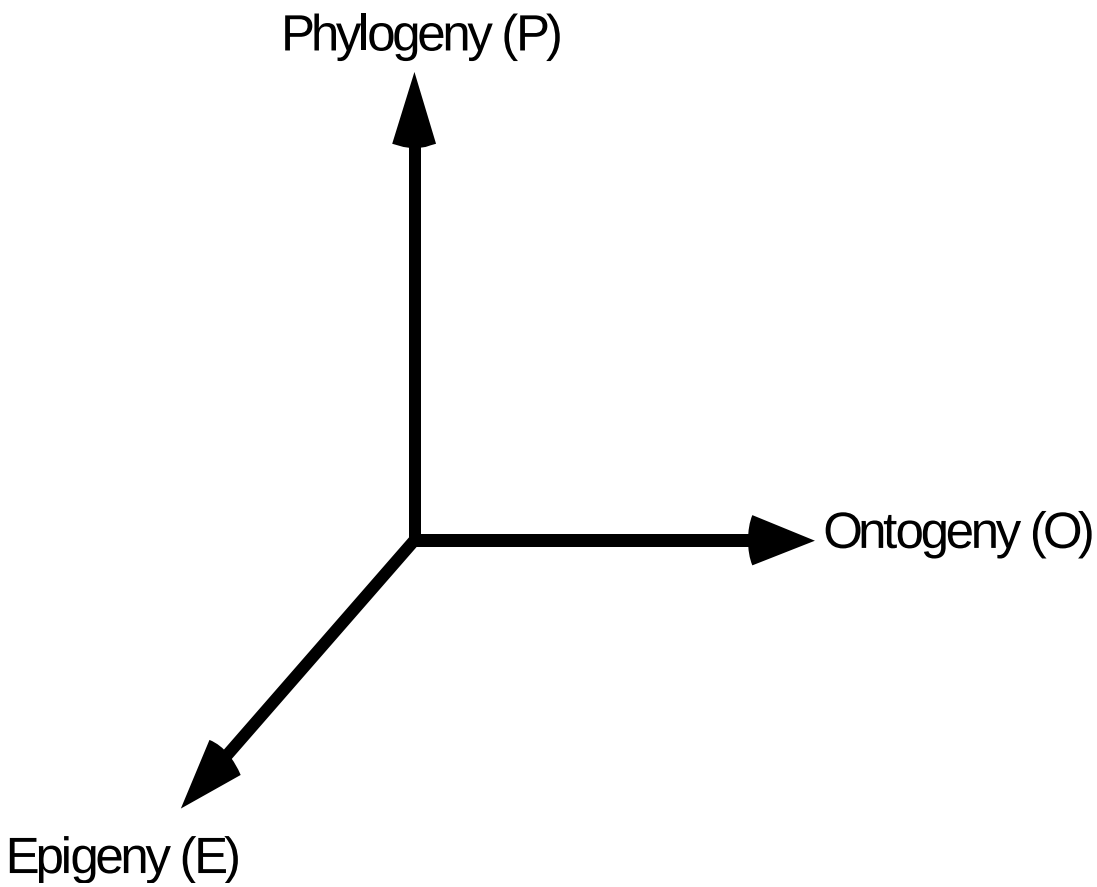
Research Interests

- Synthesis of self-checking digital circuits
- Biologically-inspired design of digital systems
- Reconfigurable computing system design
- Hardware-based molecular sequence matching

Prelude

- Very Deep Submicron technology makes VLSI-based digital systems susceptible to transient or soft errors.
- The reliability of VLSI systems can be increased by built-in fault tolerant mechanism.
- Hardware-based fault tolerance techniques result in high overhead.
- A self-healing architecture inspired by the human immune system will be presented.

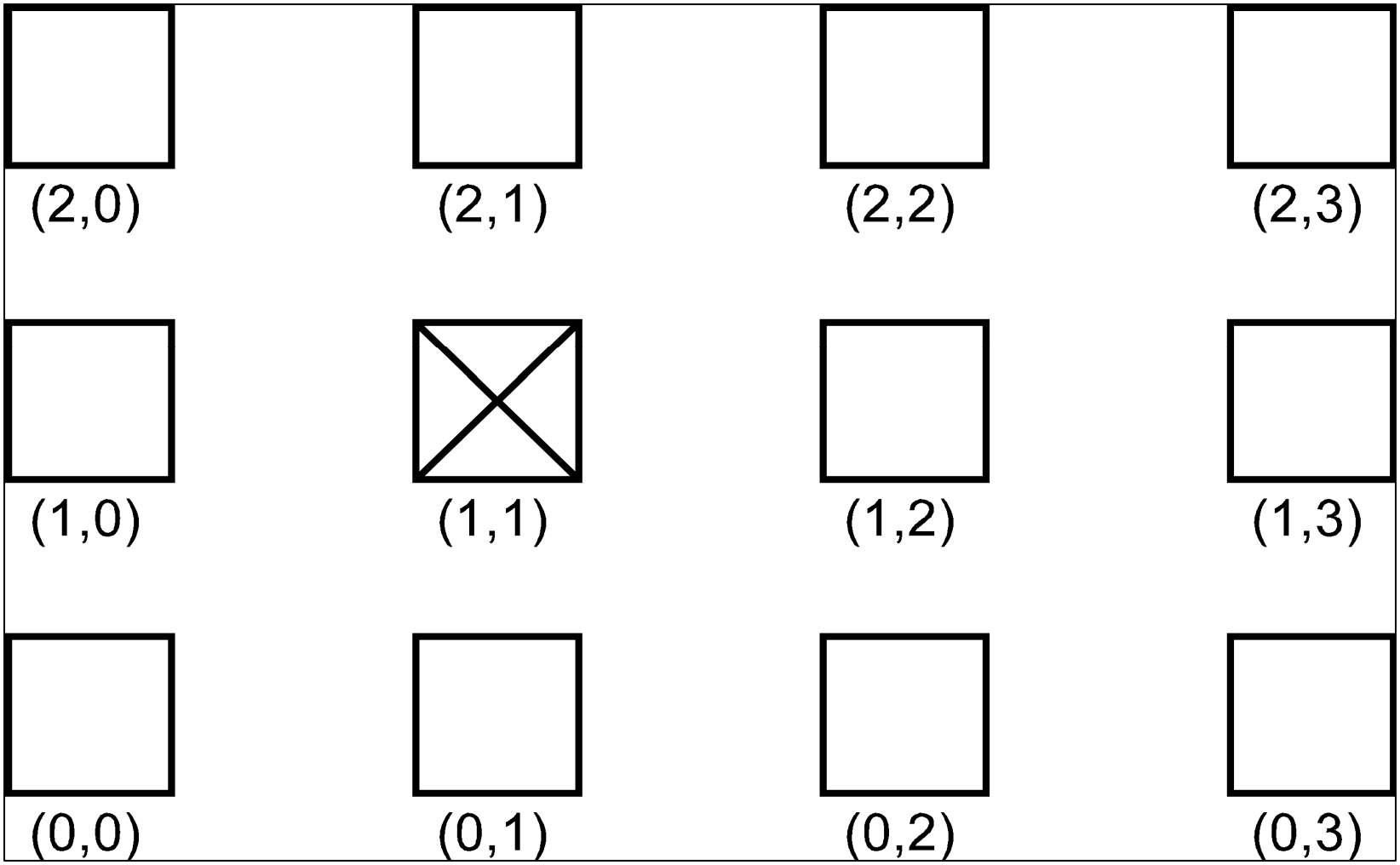
Biologically-inspired Digital System Design POE Model



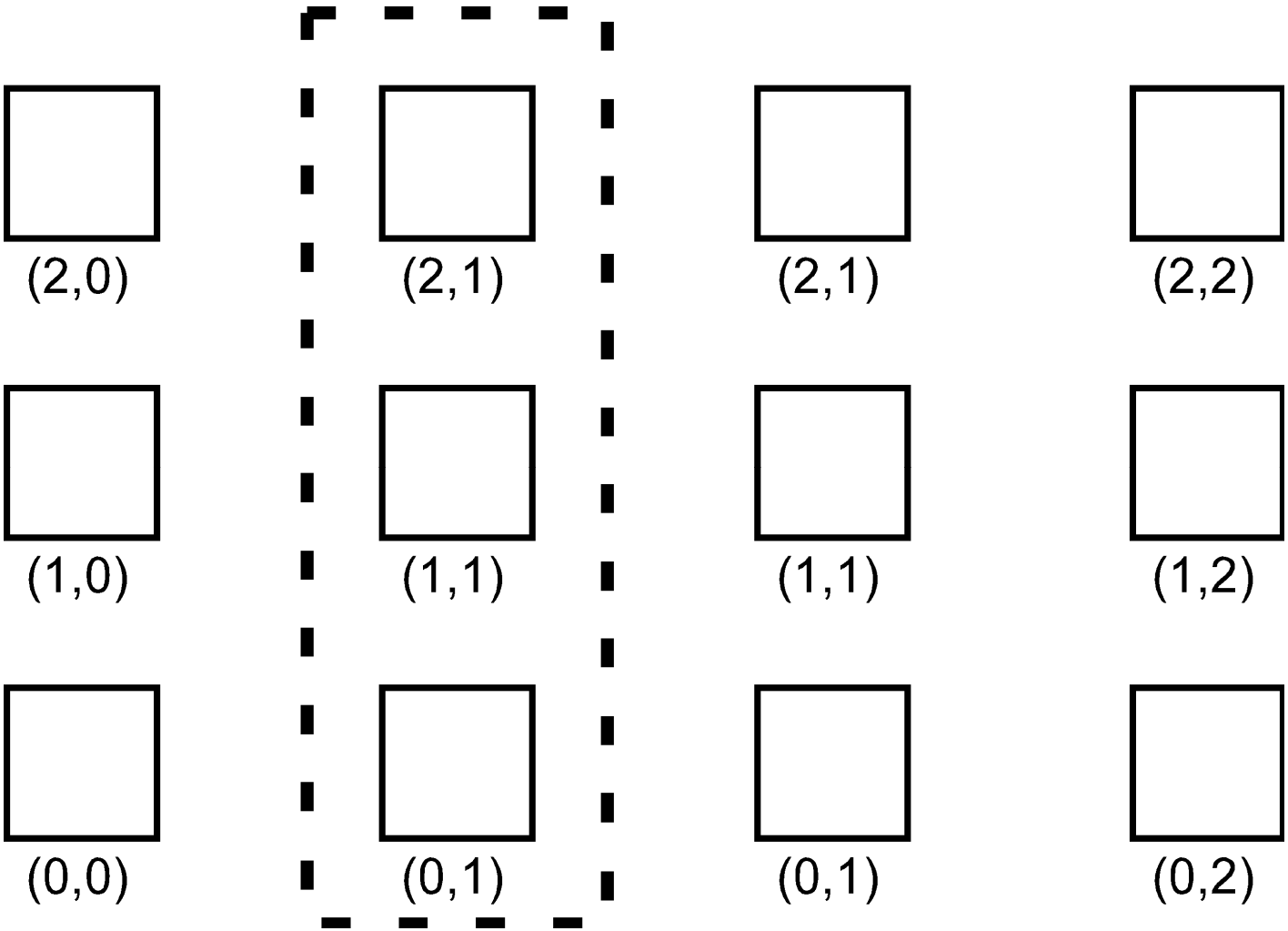
Source: " A phylogenetic , ontogenetic, and epigenetic view of bio-inspired hardware systems", M. Sipper et. al., IEEE Trans. Evol. Comput. 1997, pp.83-97

- Phylogenetic: imitates the processes involved in the evolution of organisms through time.
- Ontogenetic: behaves according to the growth of an organism from the mother cell to the adult phase
- Epigenetic: based on the theory that environment has significant influence on the growth and development of organisms

Array With A Defective Cell



Reconstructed Array



Self-healing Feature

- A self-healing system performs a recovery step to heal from a fault that is introduced in the system during normal operation.
- Self-healing design techniques have identical goals to techniques used for making a system fault- tolerant.
- Systems that use modular redundancy to tolerate one or more faulty modules might be considered to be self-healing.

Faults in Digital Circuits

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- A single stuck-at fault assumes that a signal line in a circuit is fixed to a logic 1 (stuck-at-1) or logic 0 (stuck-at-0).
- Bridging fault: Short between two or more nodes or signal lines.
- Transistor fault: A transistor is forced to conduction mode (stuck-on) or cut-off mode (stuck-off) irrespective of the gate voltage.

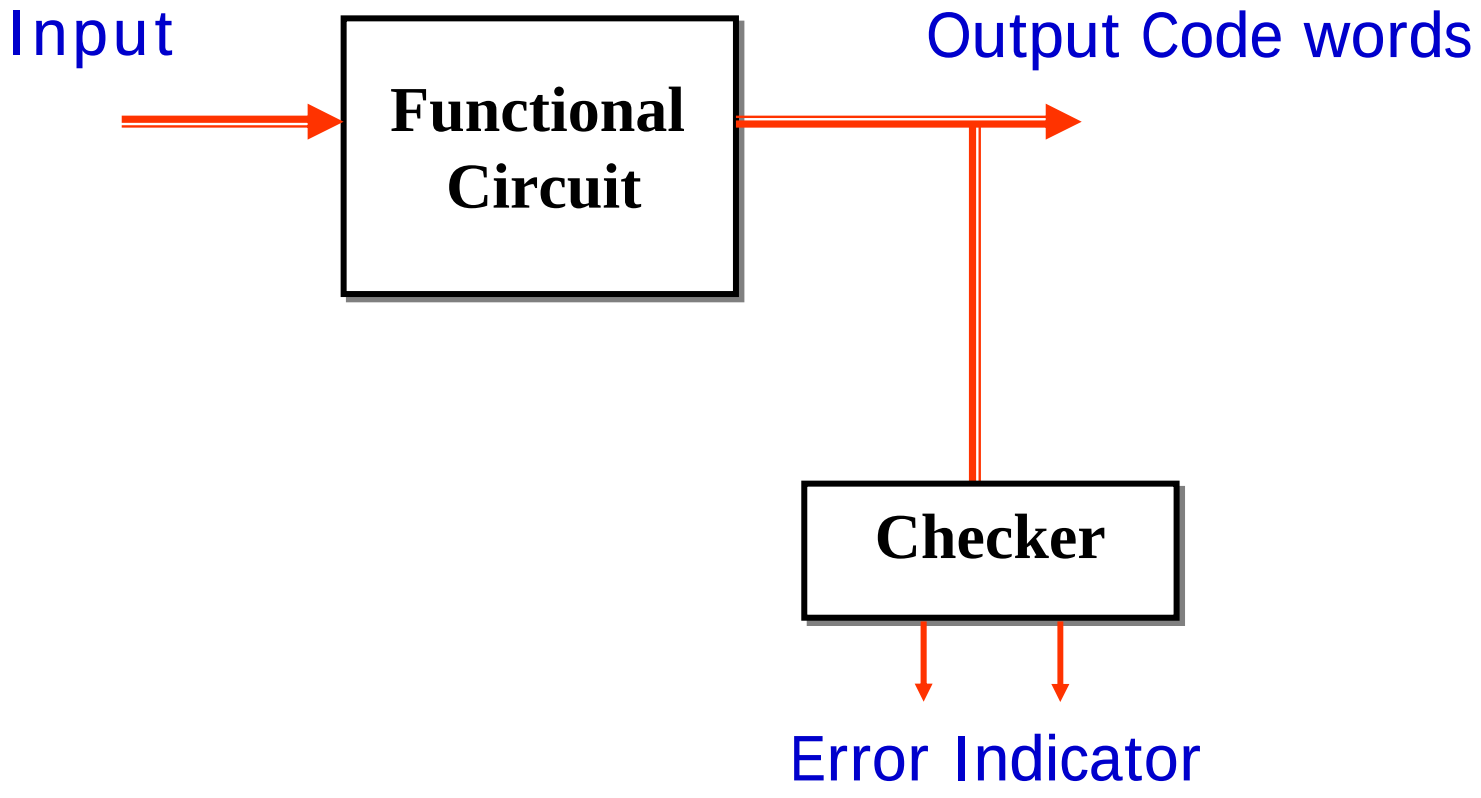
- Transient Errors: Reduction of transistor sizes adversely impacts their noise margins. Smaller transistors are more sensitive to normal radiation, noise etc.

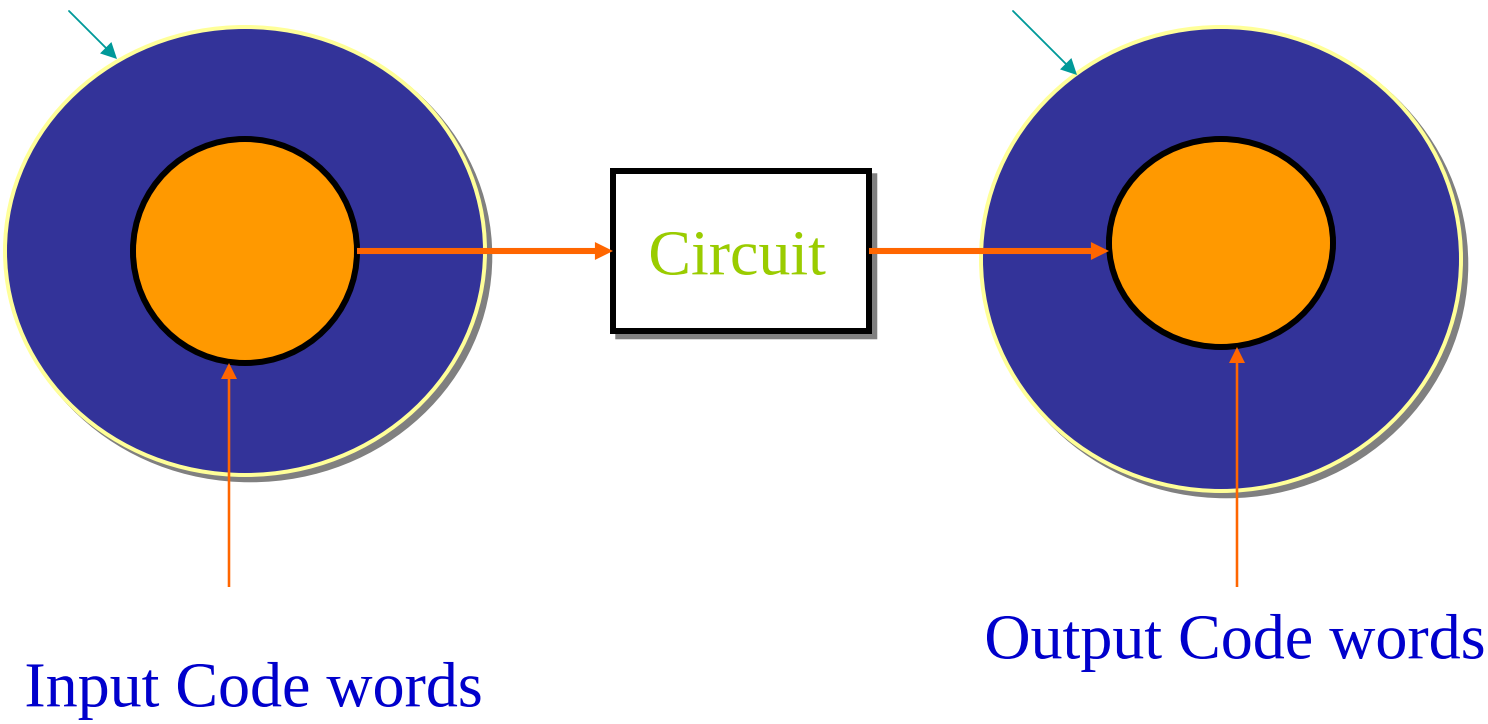
- On-line testing continuous monitoring of circuits during normal operation.

- A circuit with on-line testing capability is known as a self-checking circuit.

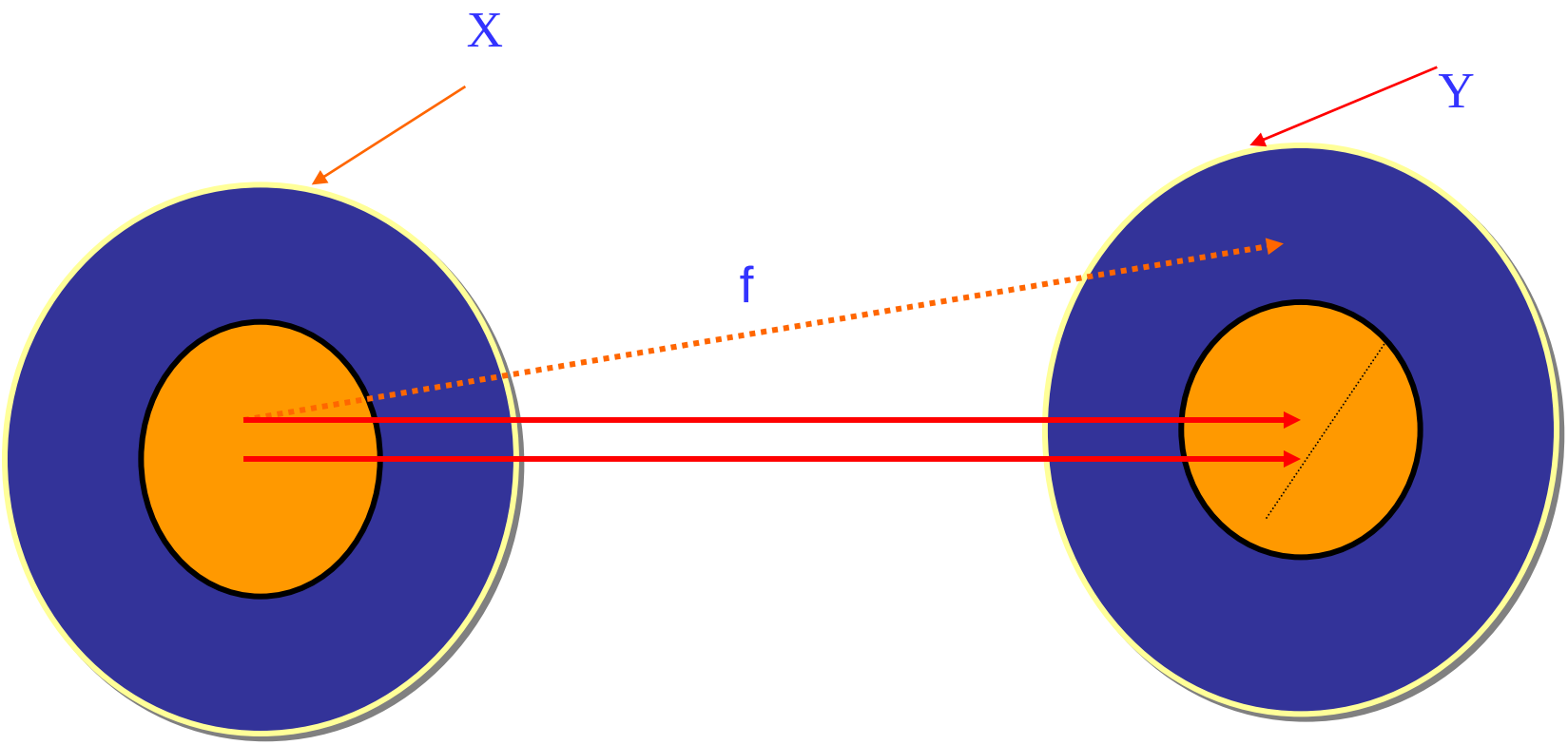
- A circuit can be designed to be self-checking only for an assumed set of faults.

Self-checking Circuit Model

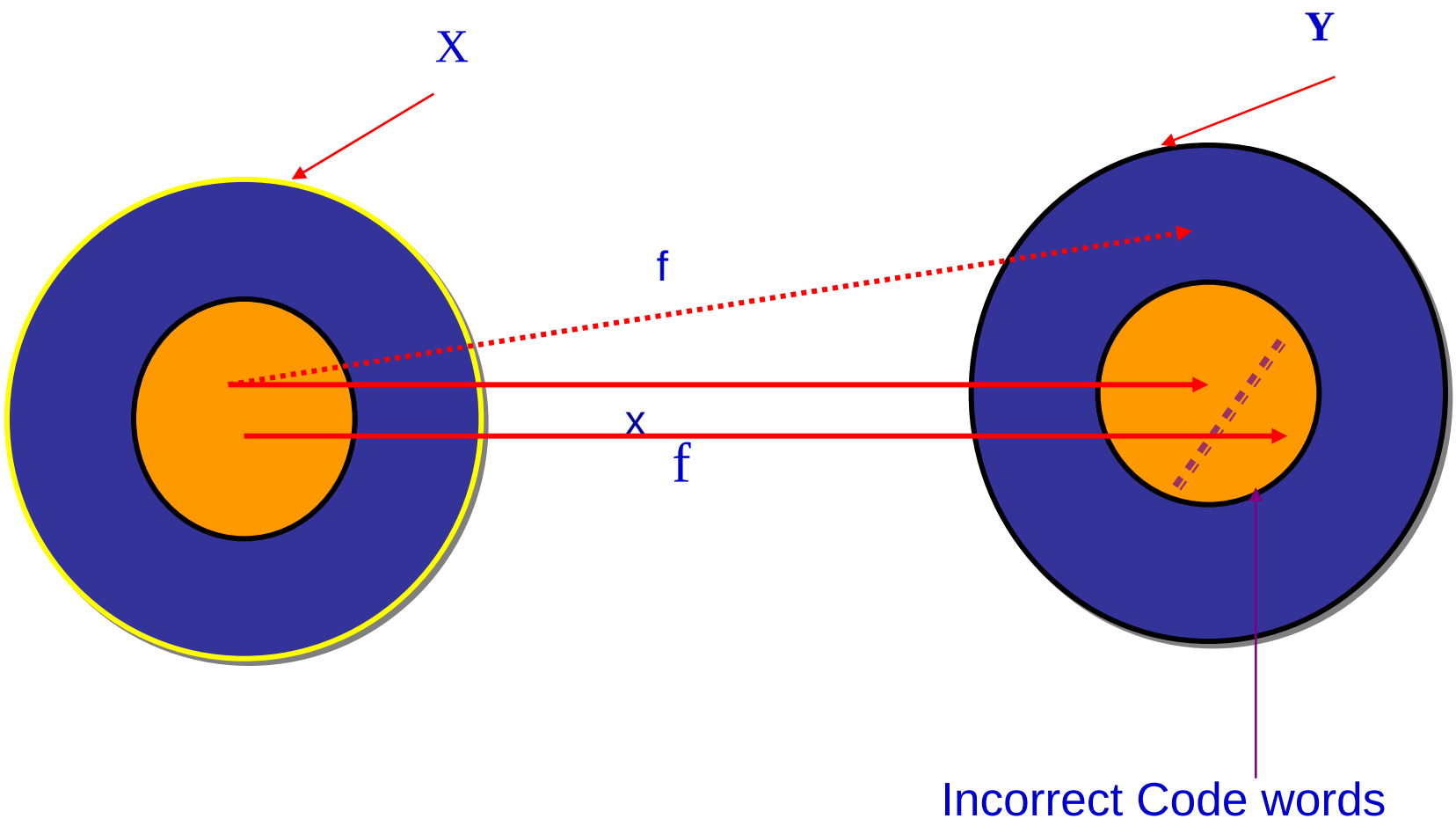



X (Input Space)
Y (Output Space)
Circuit
Input Code words
Output Code words

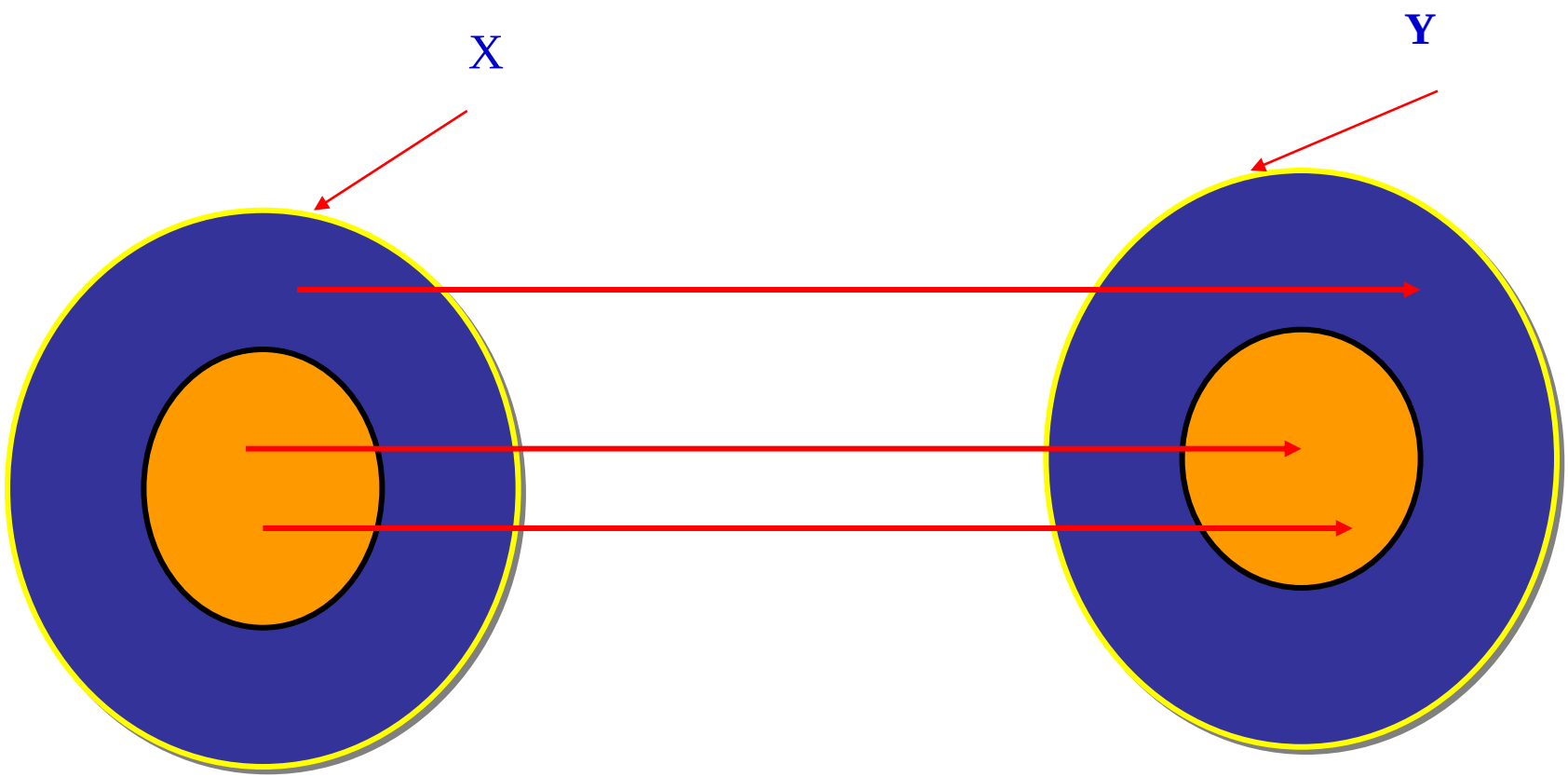
Self-testing: for every fault in a set the circuit produces a non-code word output for at least one input code word



Fault secure: the output will either be a non-code word or a correct code word in the presence of a fault from a specified set.



Code-disjoint: the output will be a valid code word if and only if the input is a code word.



Error Detecting Codes

Error Detecting Codes

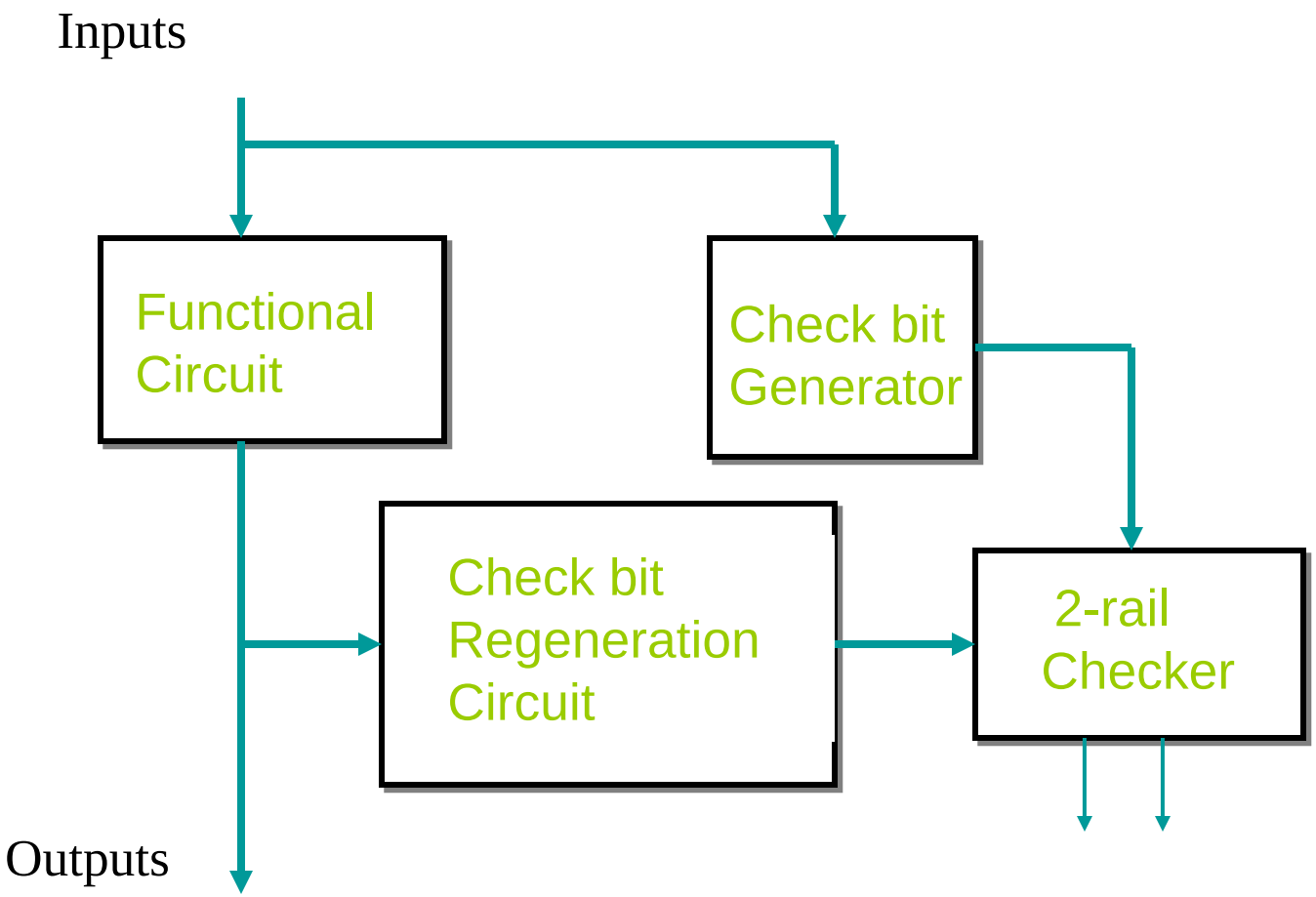
Separable Codes

- Parity Code
- Berger Code
- Residue Code

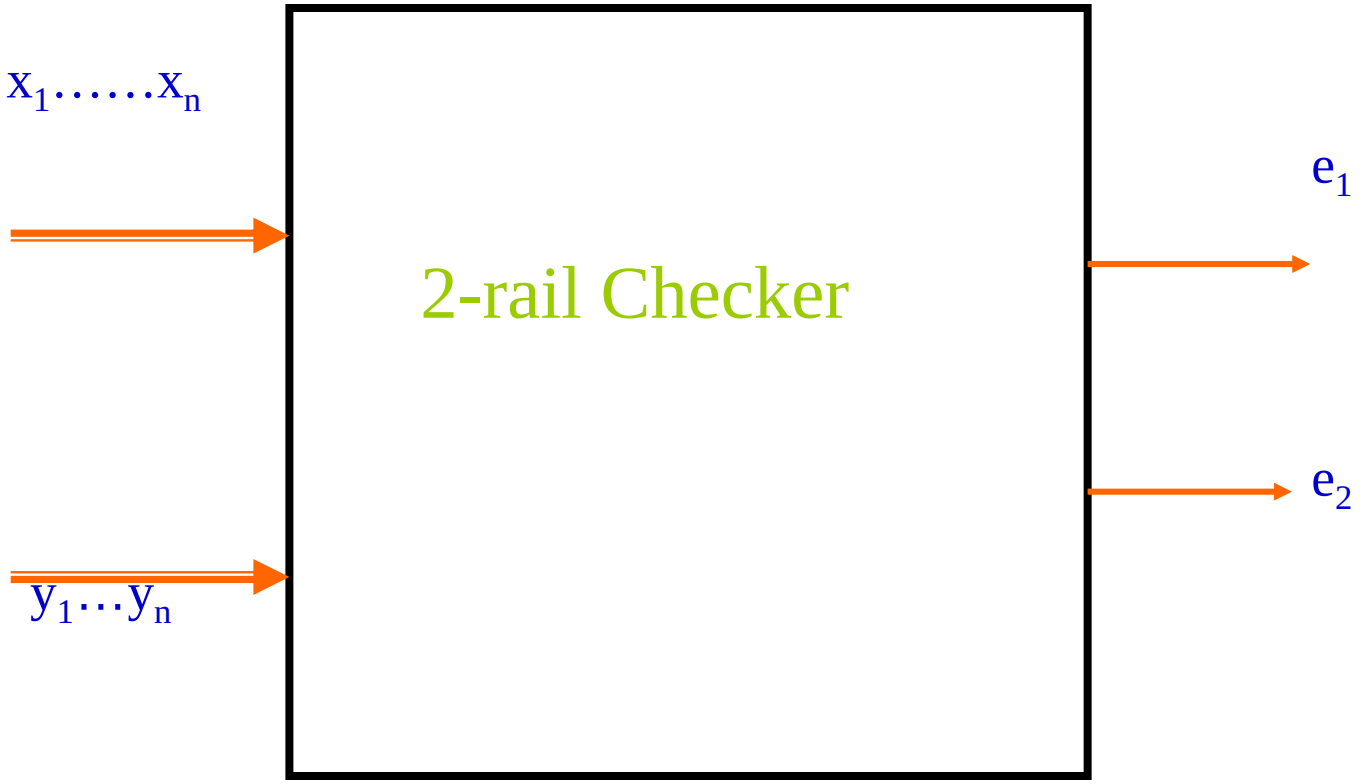
Non-separable Codes

- m-out-of-n Code

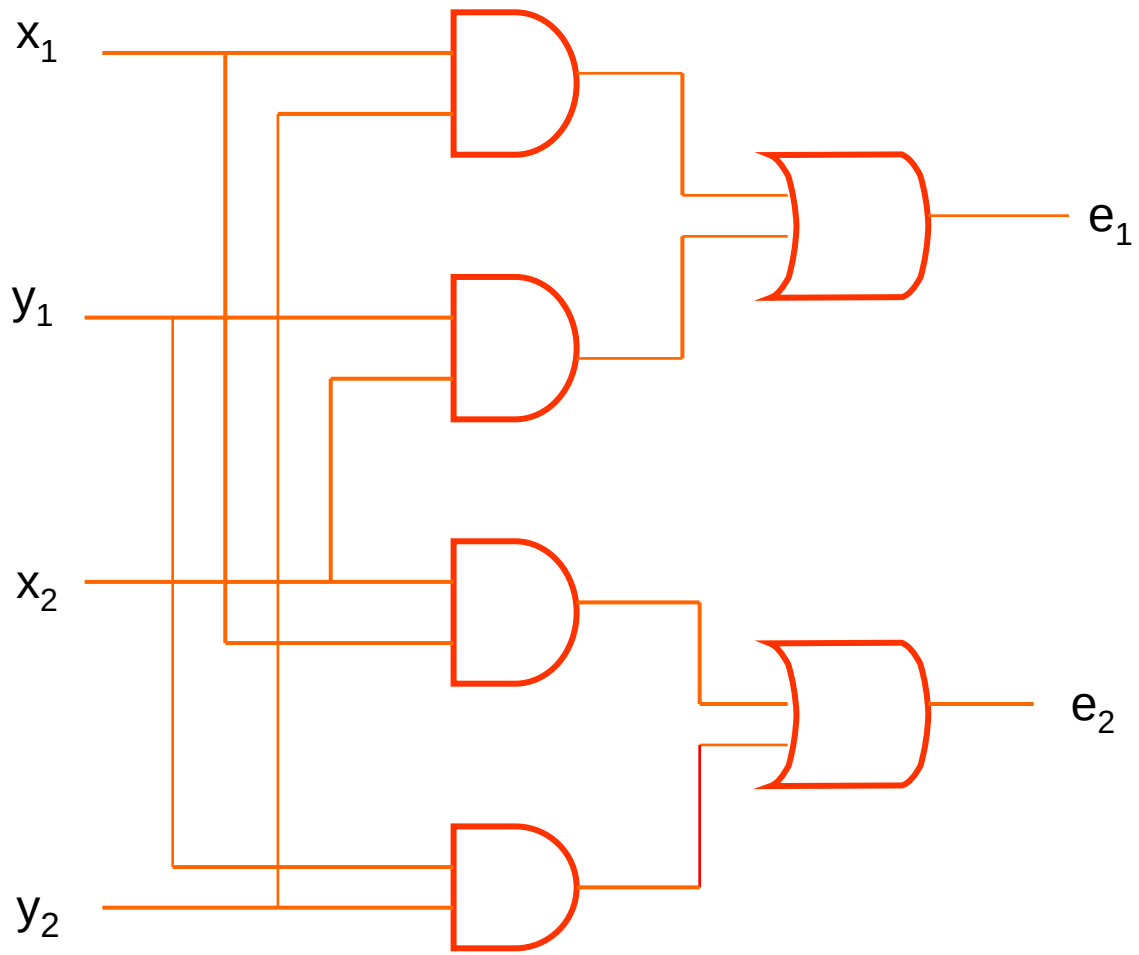
Self-checking Circuit with Separable Codes



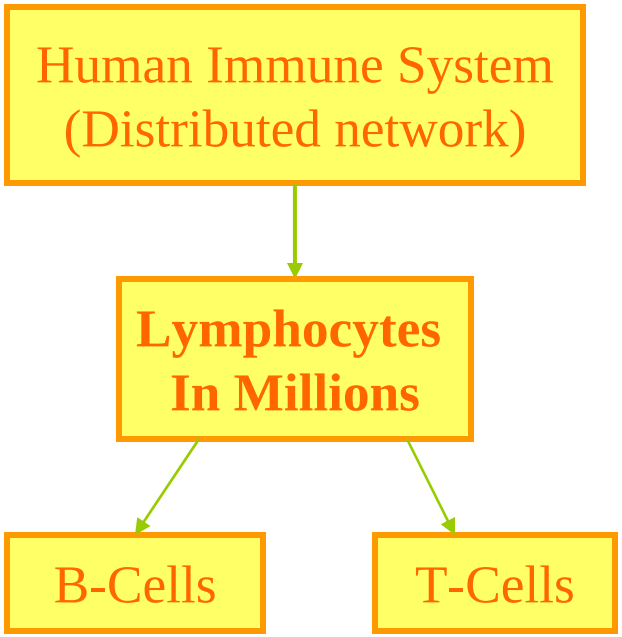
Two-rail Checker



Two-bit 2-rail Checker



Overview of Human Immune System

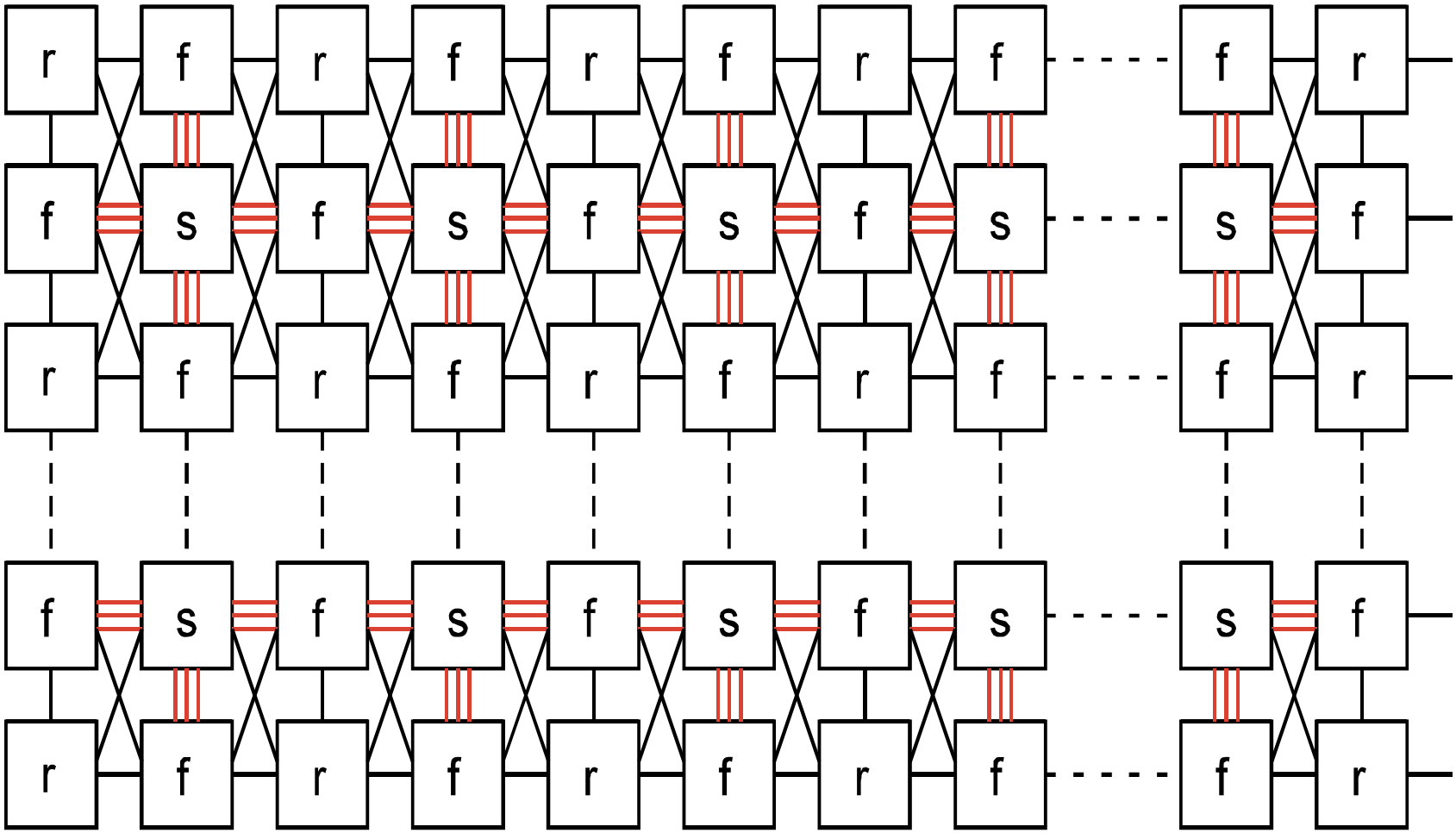


- The immune system works without any central command and is distributed
  - B cells : recognize and lock the antigens
  - T cells : eliminate locked antigens

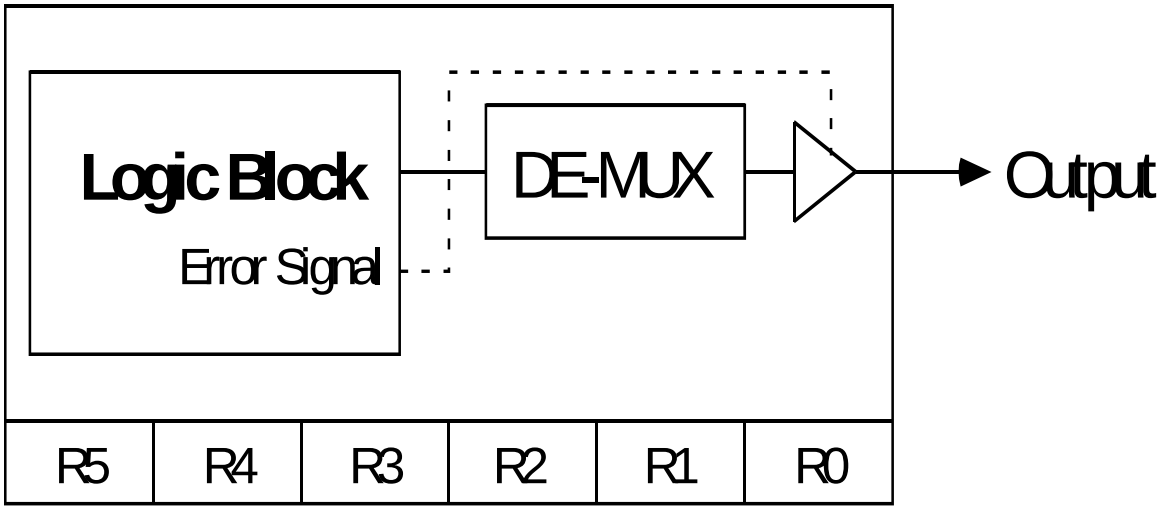
Features of the Proposed System Architecture

- This architecture like the human immune system is a distributed network without any centralized control.
- Fault (antigen) detection is based on the principle of operation of the B-cell.
- Once a fault is detected in a functional cell, a pre-selected spare cell replaces the functional cell by cloning its behavior

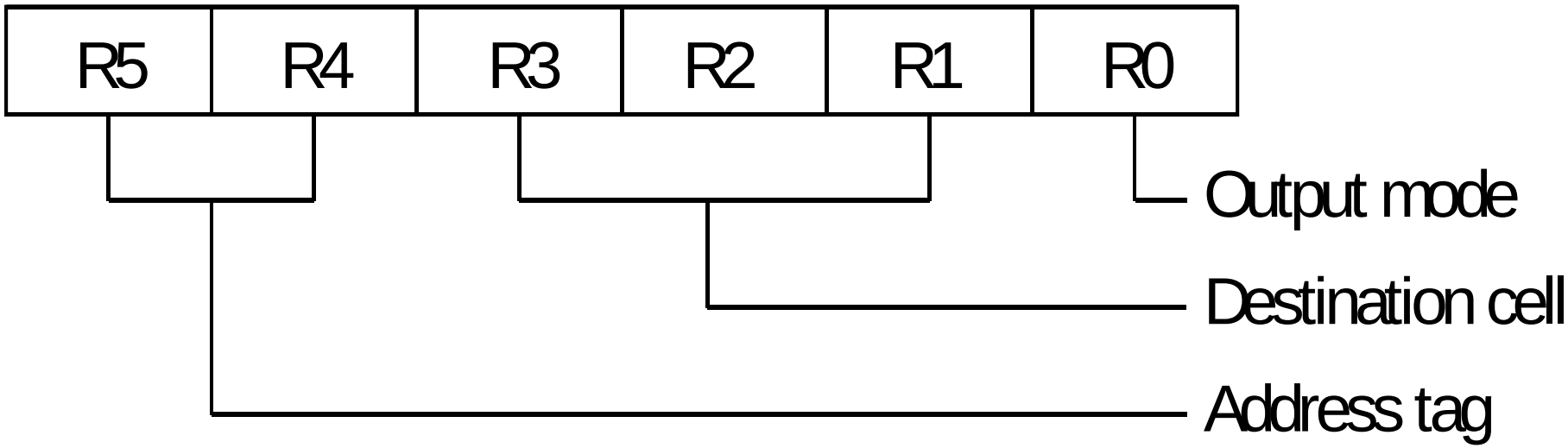
Self-healing Architecture



- Functional cell consists of a 3-input/1-output logic block, a 6-bit control register and an error register
- The logic block can perform any logical operation of three variables

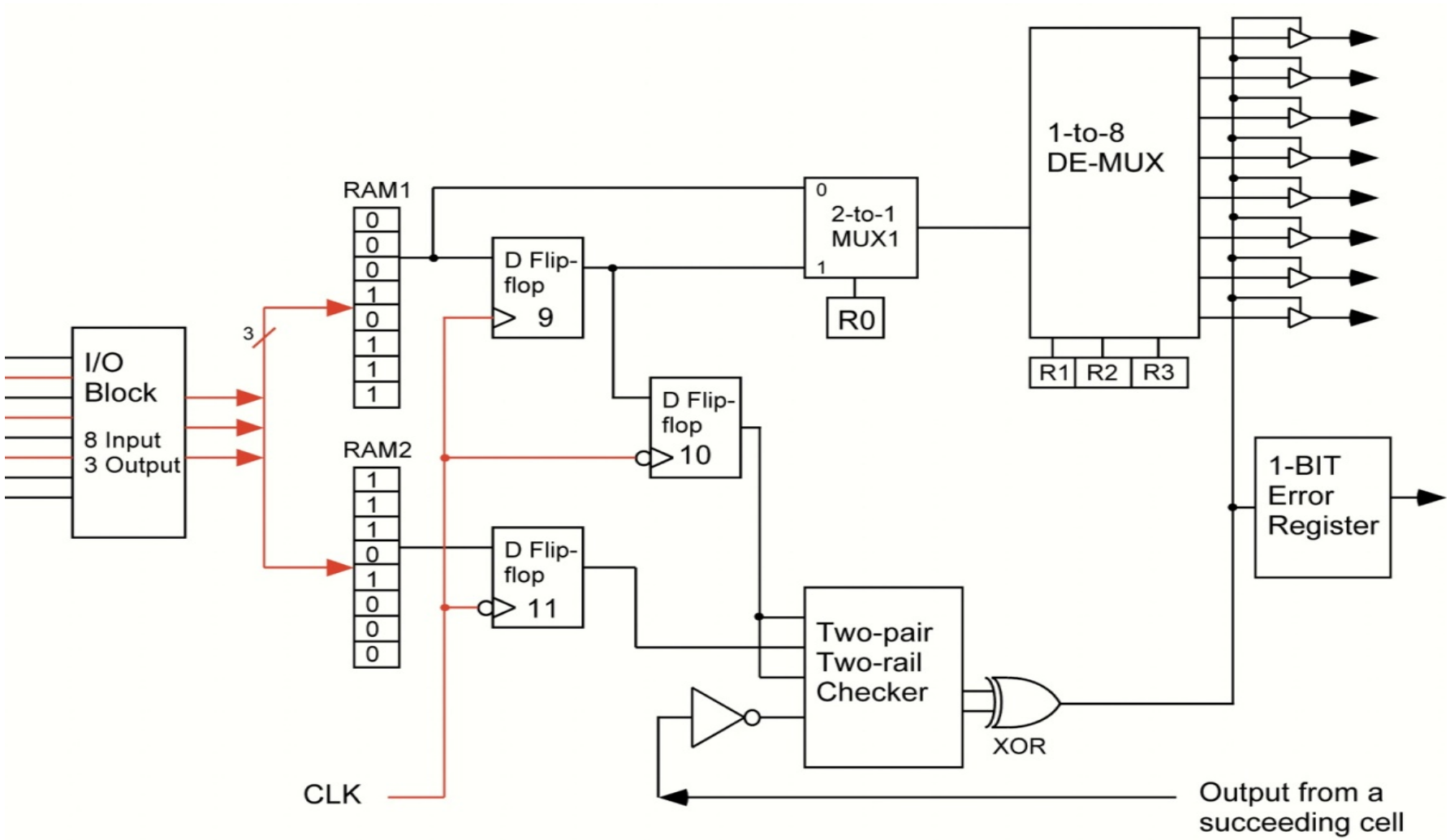


Control Register



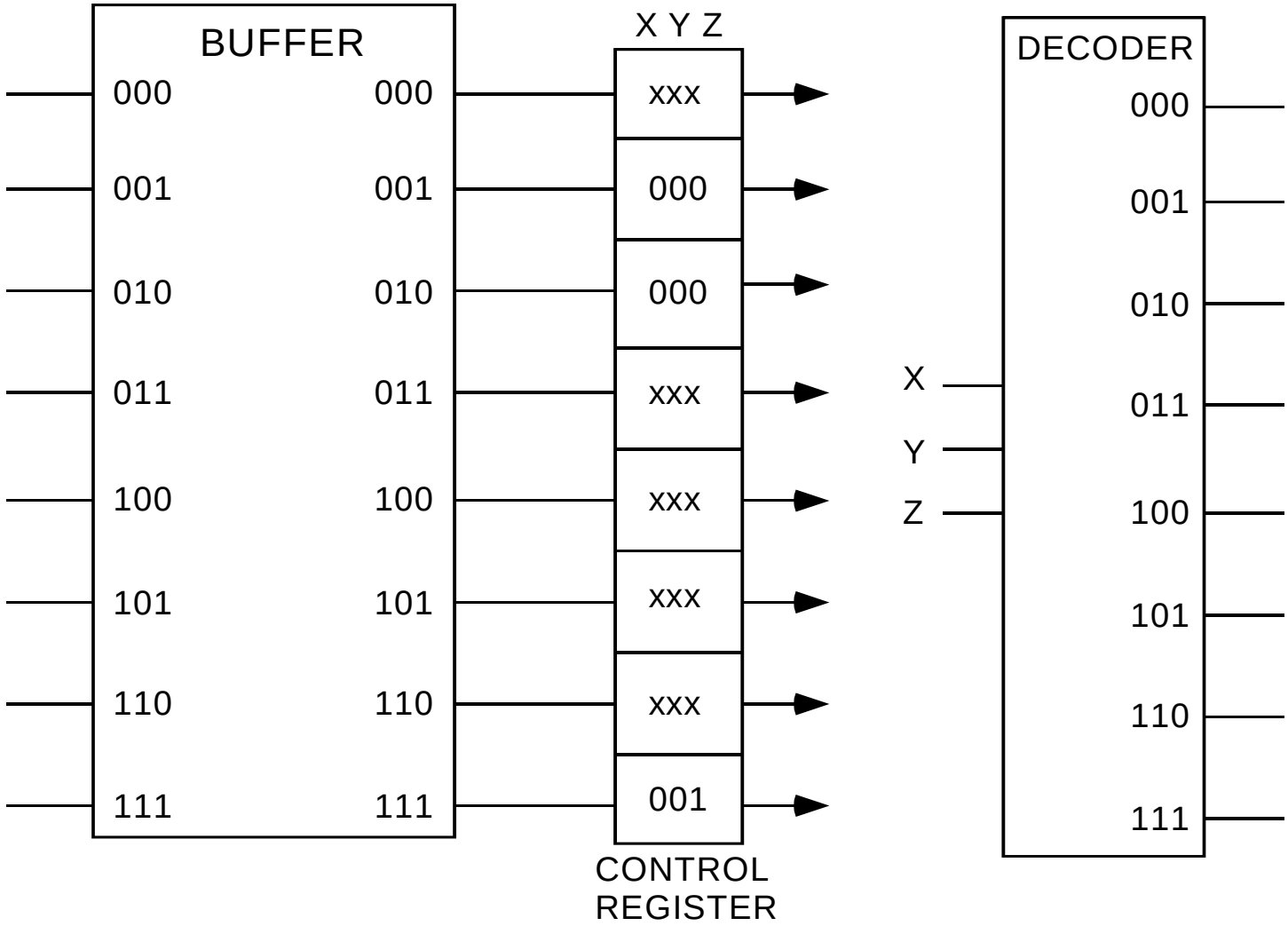
- All functional cells in the architecture are programmable using the control register.
- By changing the contents of the RAM in the logic block and the control register, the same functional cell can be made to perform different functions.

Functional Cell

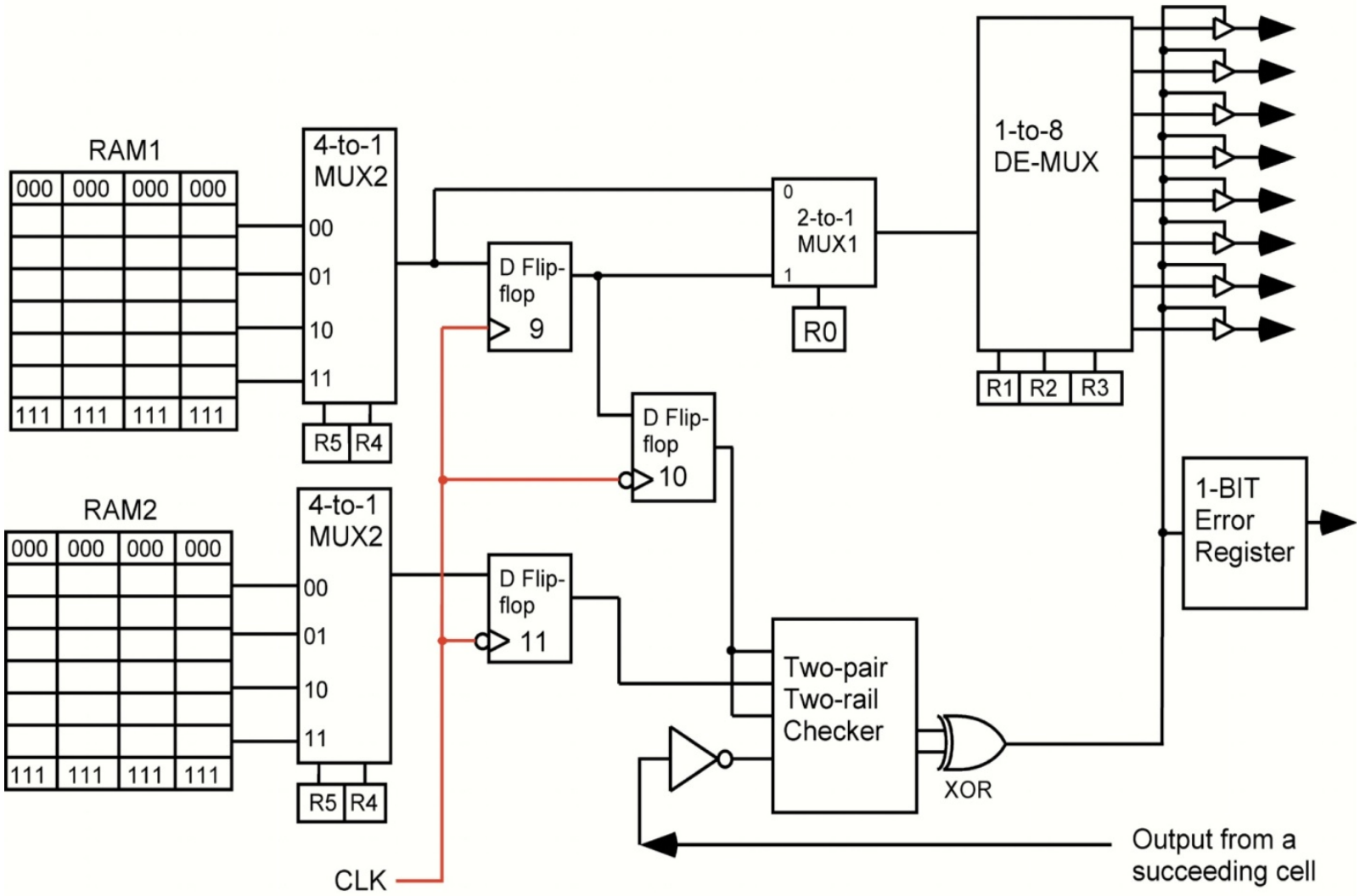


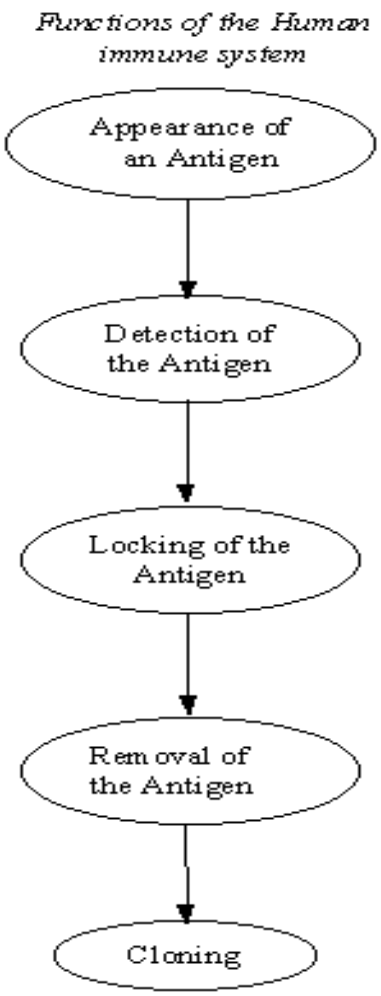
- The outputs generated by the RAMs are complementary.
- If the outputs are identical, the results are forced in to a high impedance state.
- By forcing the outputs of a functional cell to 00 or 11 in the presence of an error, the role of a B cell is emulated.
- If an error is detected the 1-bit error register in the cell is set to 0; the inputs to the cell are transferred into the adjacent spare cell

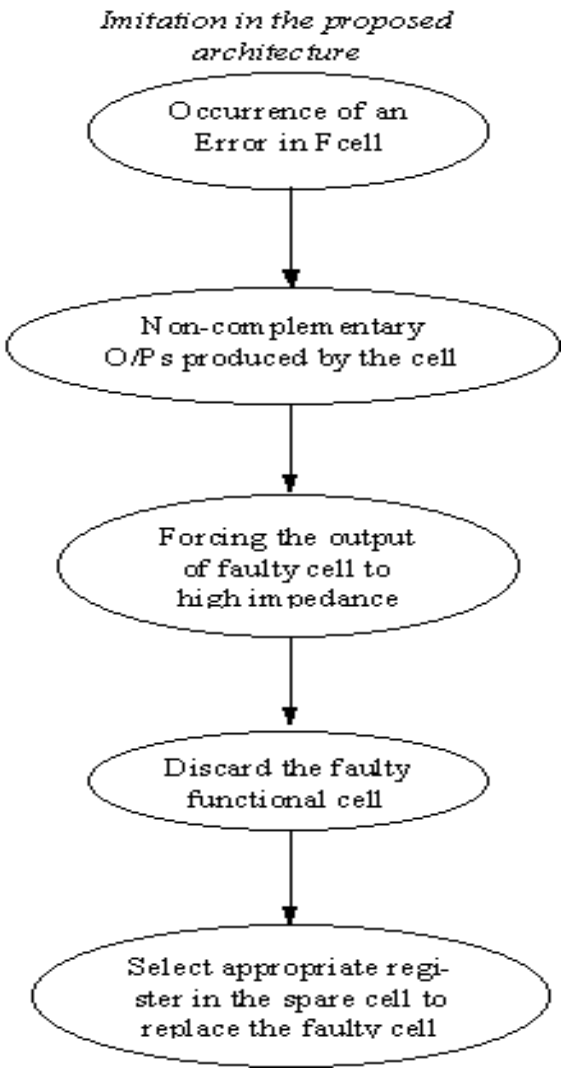
Router Cell


BUFFER
000
001
010
011
100
101
110
111
000
001
010
011
100
101
110
111
X Y Z
xxx
000
000
xxx
xxx
xxx
xxx
001
CONTROL
REGISTER
DECODER
X
Y
Z
000
001
010
011
100
101
110
111

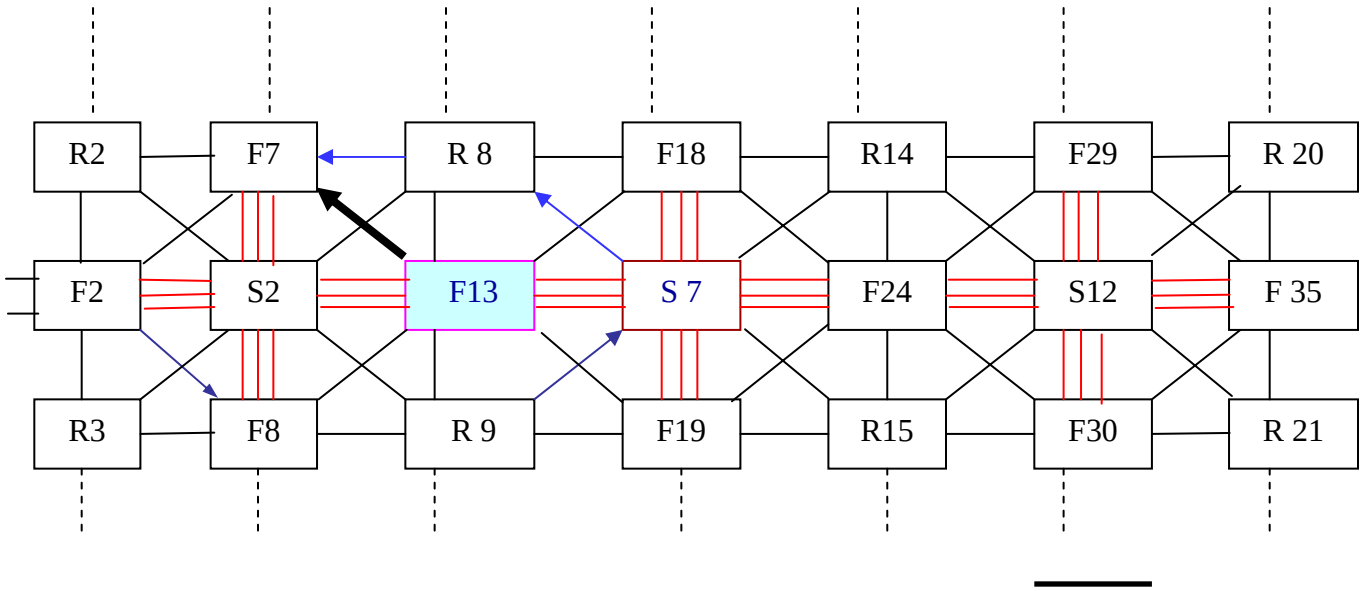
Spare Cell


RAM1
000 000 000 000
111 111 111 111
4-to-1 MUX2
00
01
10
11
R5 R4
RAM2
000 000 000 000
111 111 111 111
4-to-1 MUX2
00
01
10
11
R5 R4
D Flip-flop 9
D Flip-flop 10
D Flip-flop 11
0
2-to-1 MUX1
1
R0
1-to-8 DE-MUX
R1 R2 R3
1-BIT Error Register
Two-pair Two-rail Checker
XOR
Output from a succeeding cell
CLK


Functions of the Human immune system
Appearance of an Antigen
Detection of the Antigen
Locking of the Antigen
Removal of the Antigen
Cloning

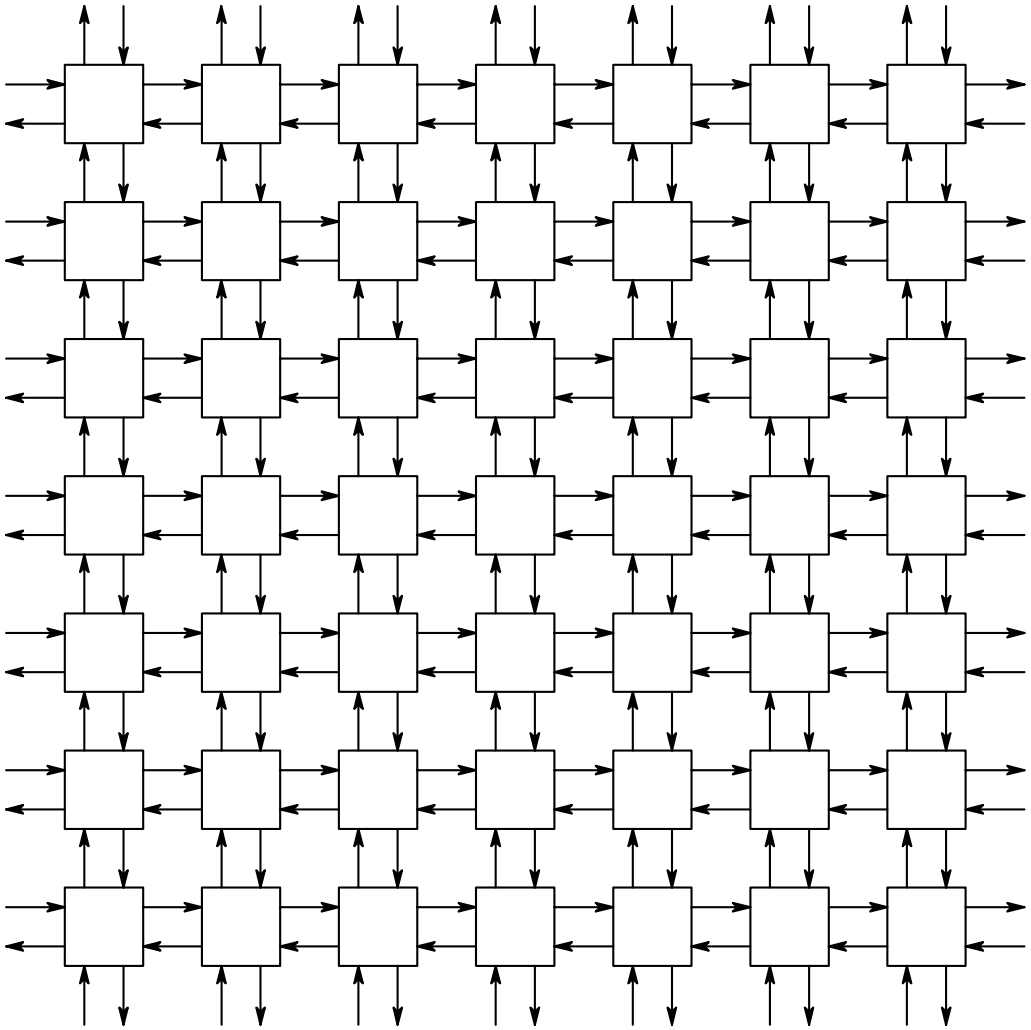

Imitation in the proposed architecture
Occurrence of an Error in F cell
Non-complementary O/Ps produced by the cell
Forcing the output of faulty cell to high impedance
Discard the faulty functional cell
Select appropriate register in the spare cell to replace the faulty cell

Example of Self-healing

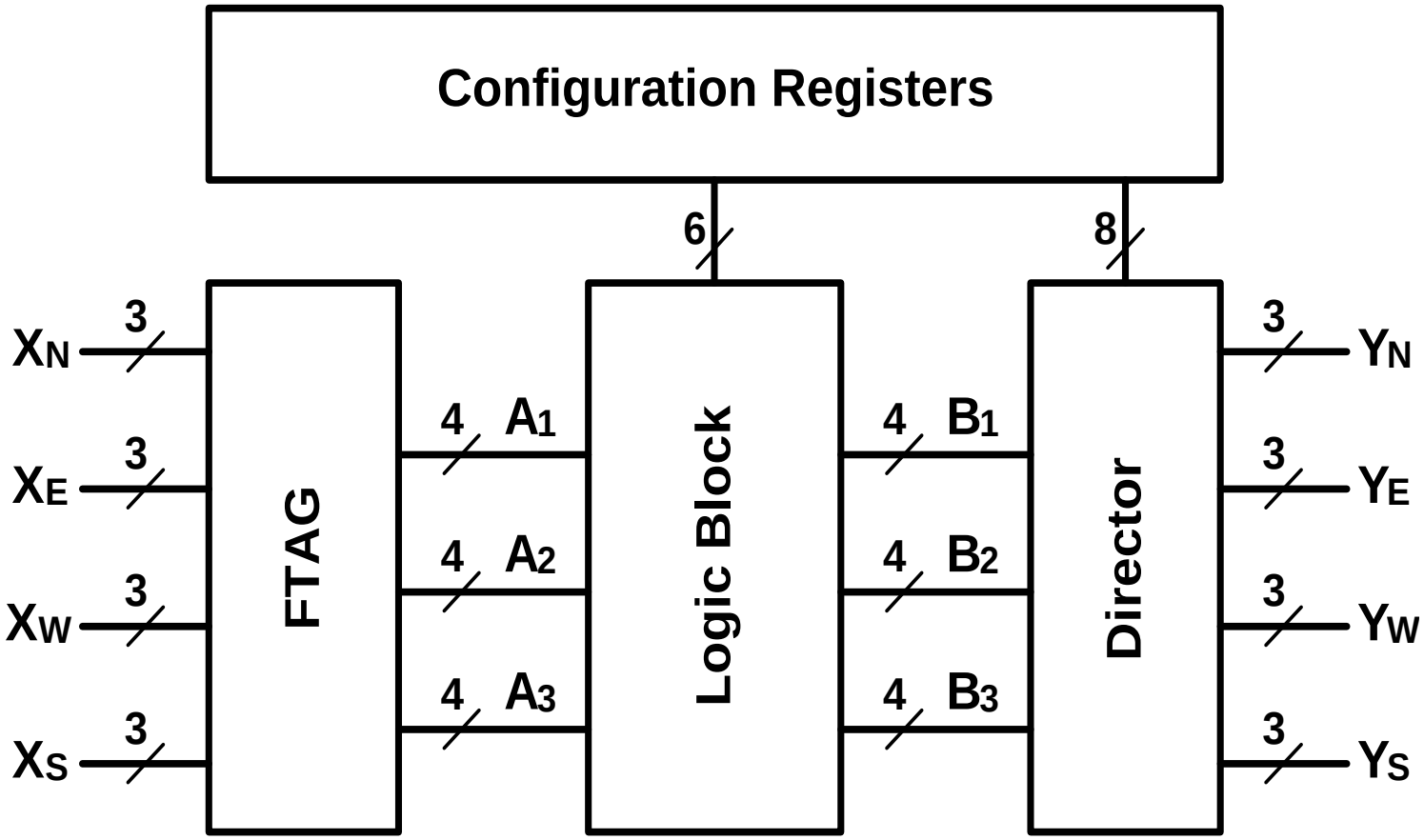


- Assume a fault in functional cell F13; the outputs of the cell are 00 and 11 i.e. not complementary
- The tag bits for F13 are decoded, and the control register corresponding to F13 is activated in spare cell S7
- The circuit continues its normal operation.

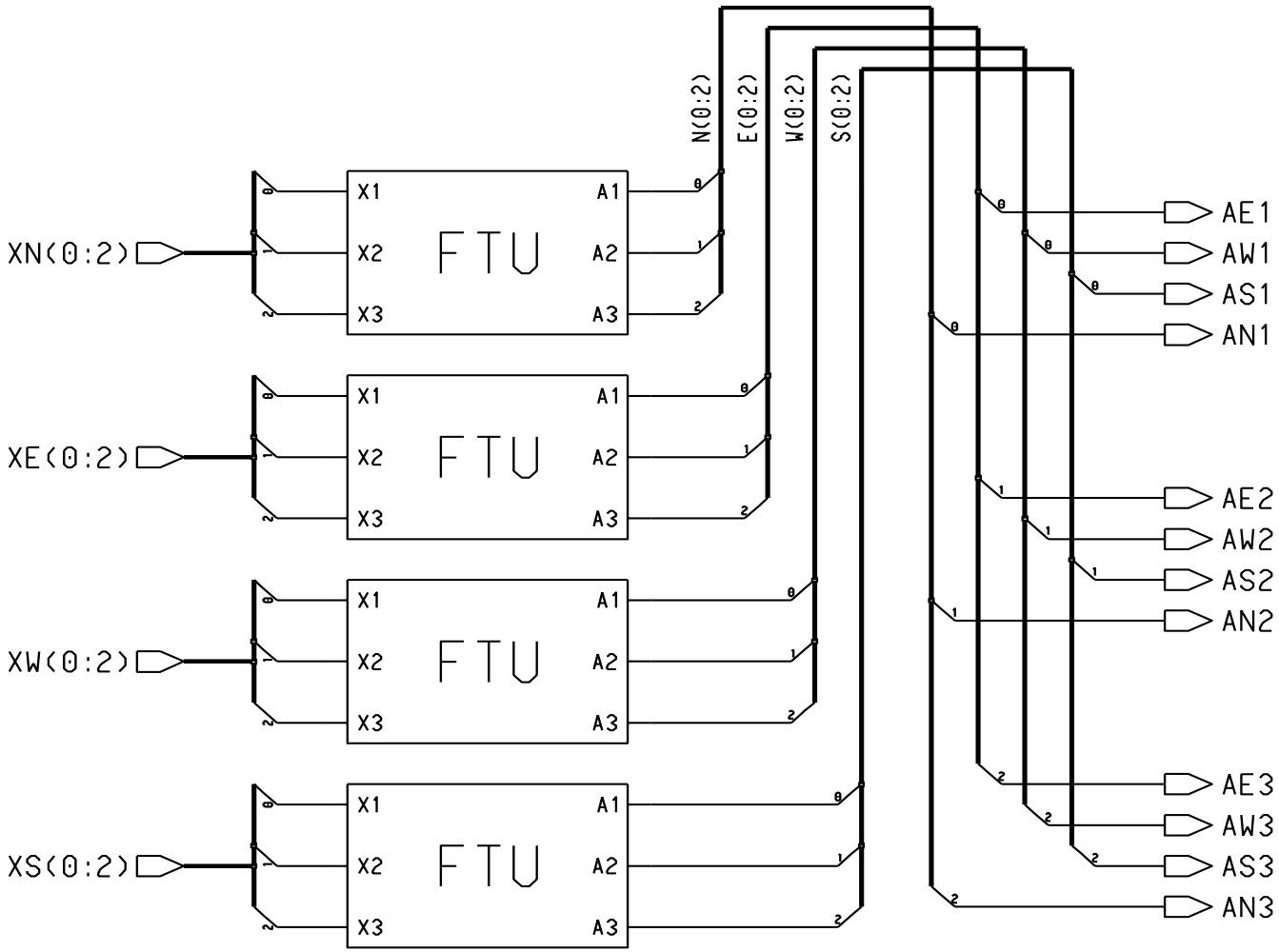
New FPGA Architecture



Fault Tolerant Functional Cell



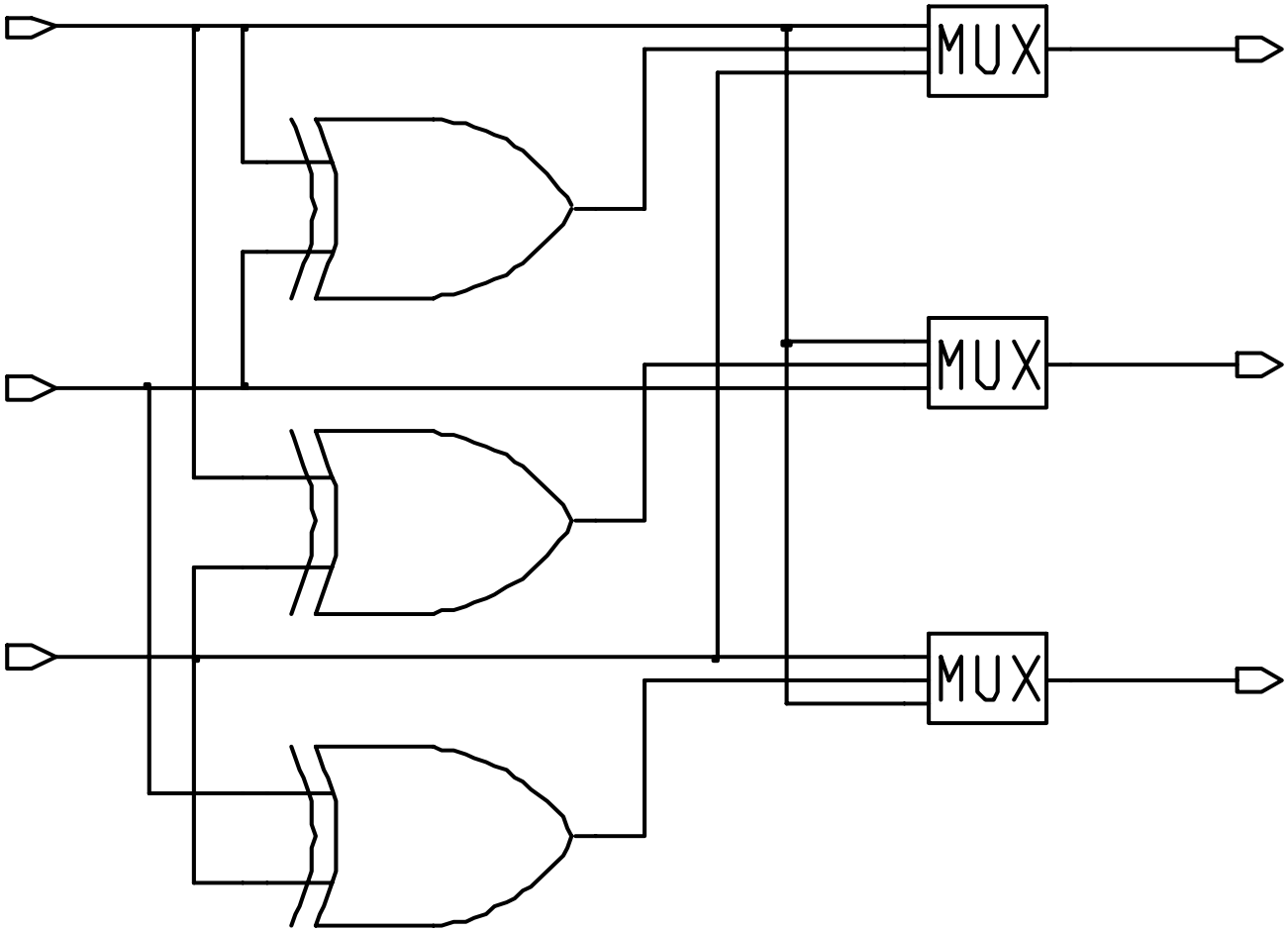
Fault Tolerant Address Generator



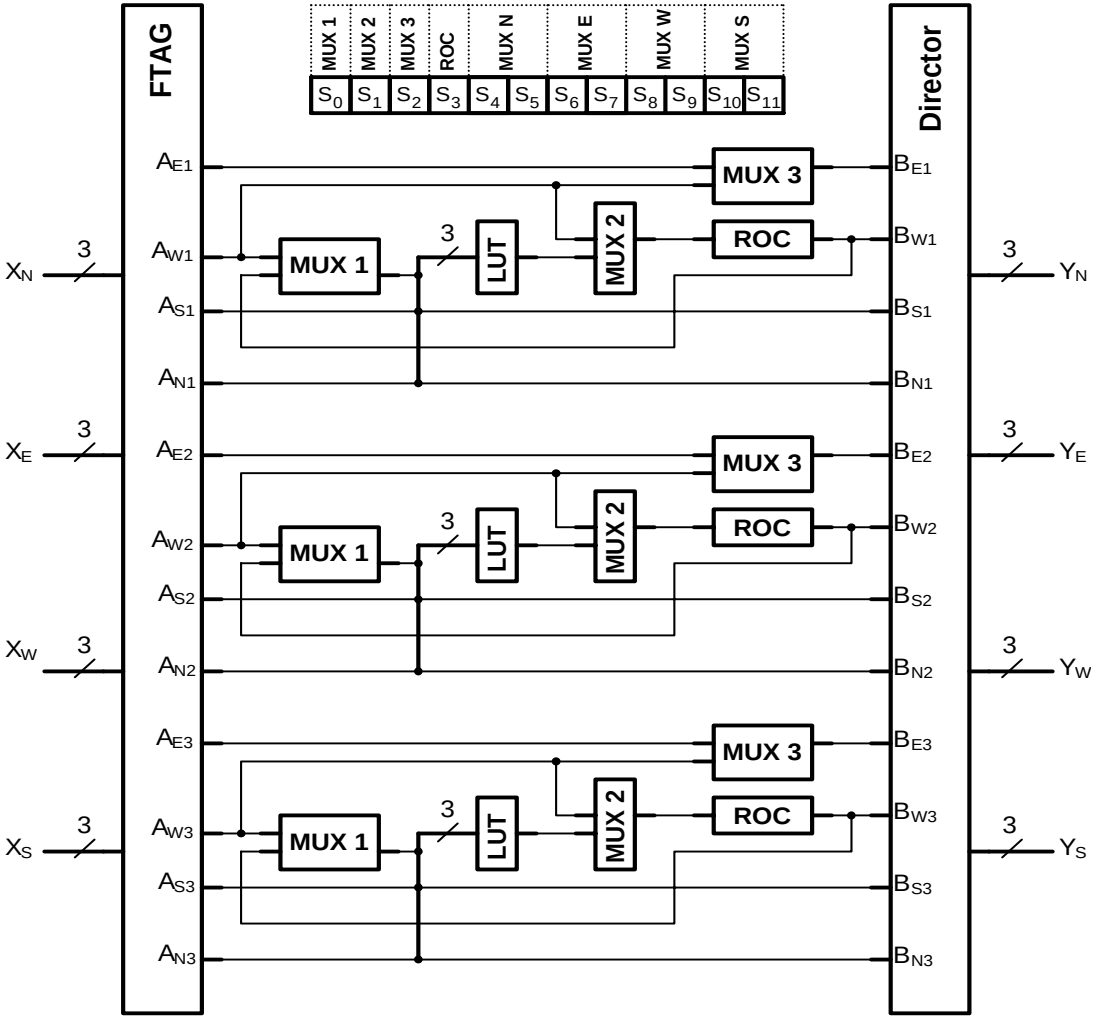
Similarity Checker

Inputs			*Outputs*			*Result*
A	B	C	D = {AB}	E = {AC}	F = {BC}	
0	0	0	A/B	A/C	B/C	0
0	0	1	A/B	B	A	0
0	1	0	C	A/C	A	0
0	1	1	C	B	B/C	1
1	0	0	C	B	B/C	0
1	0	1	C	A/C	A	1
1	1	0	A/B	B	A	1
1	1	1	A/B	A/C	B/C	1

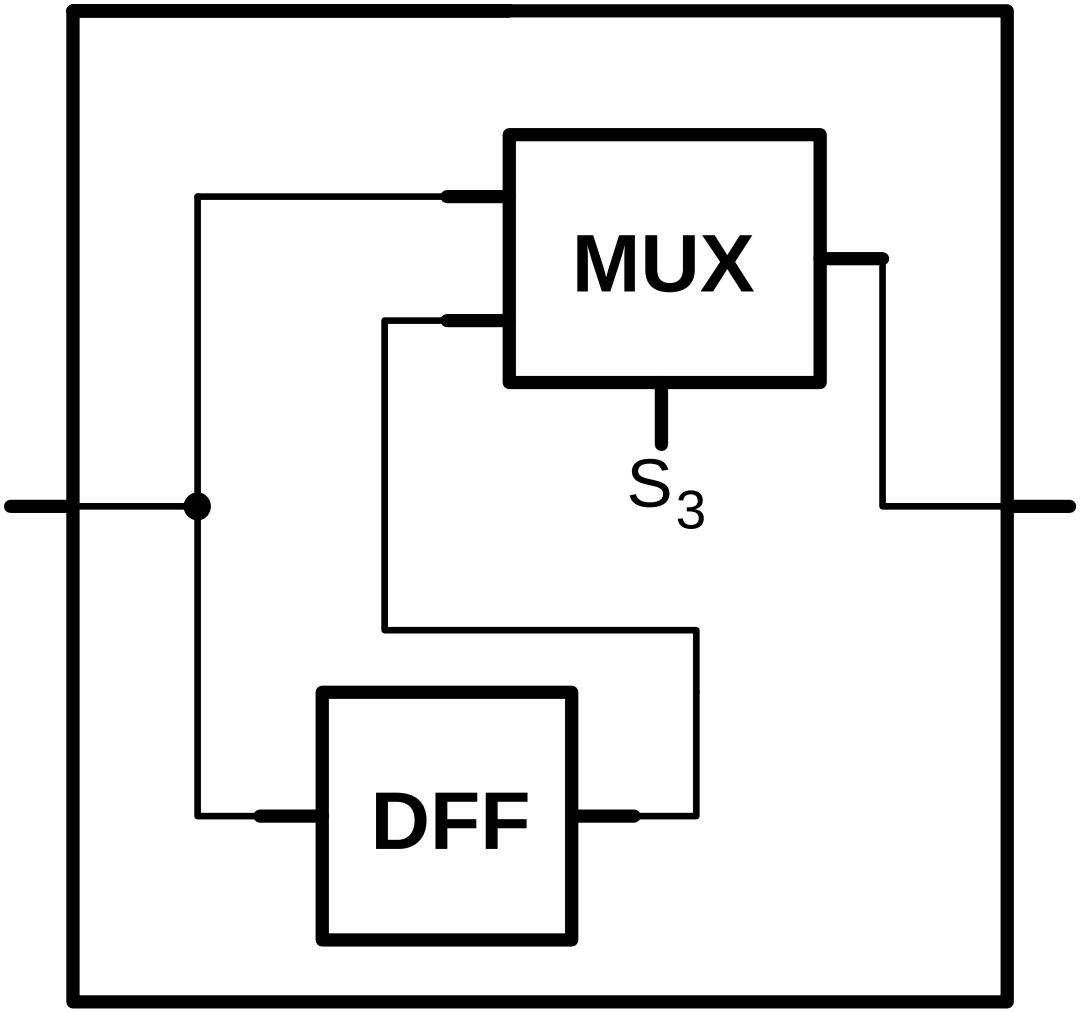
Similarity Checker Circuit



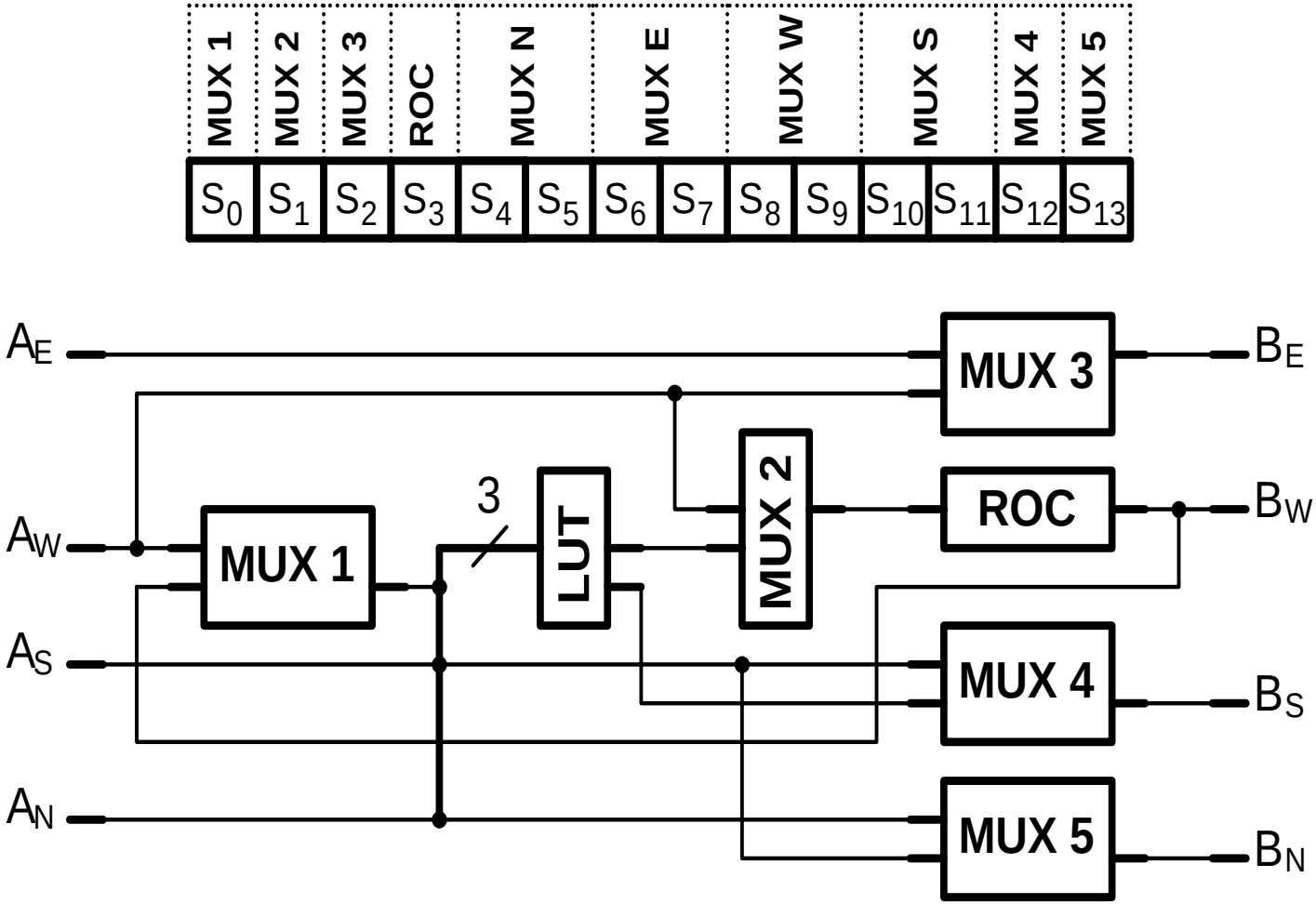
Logic Block with Three LUTs



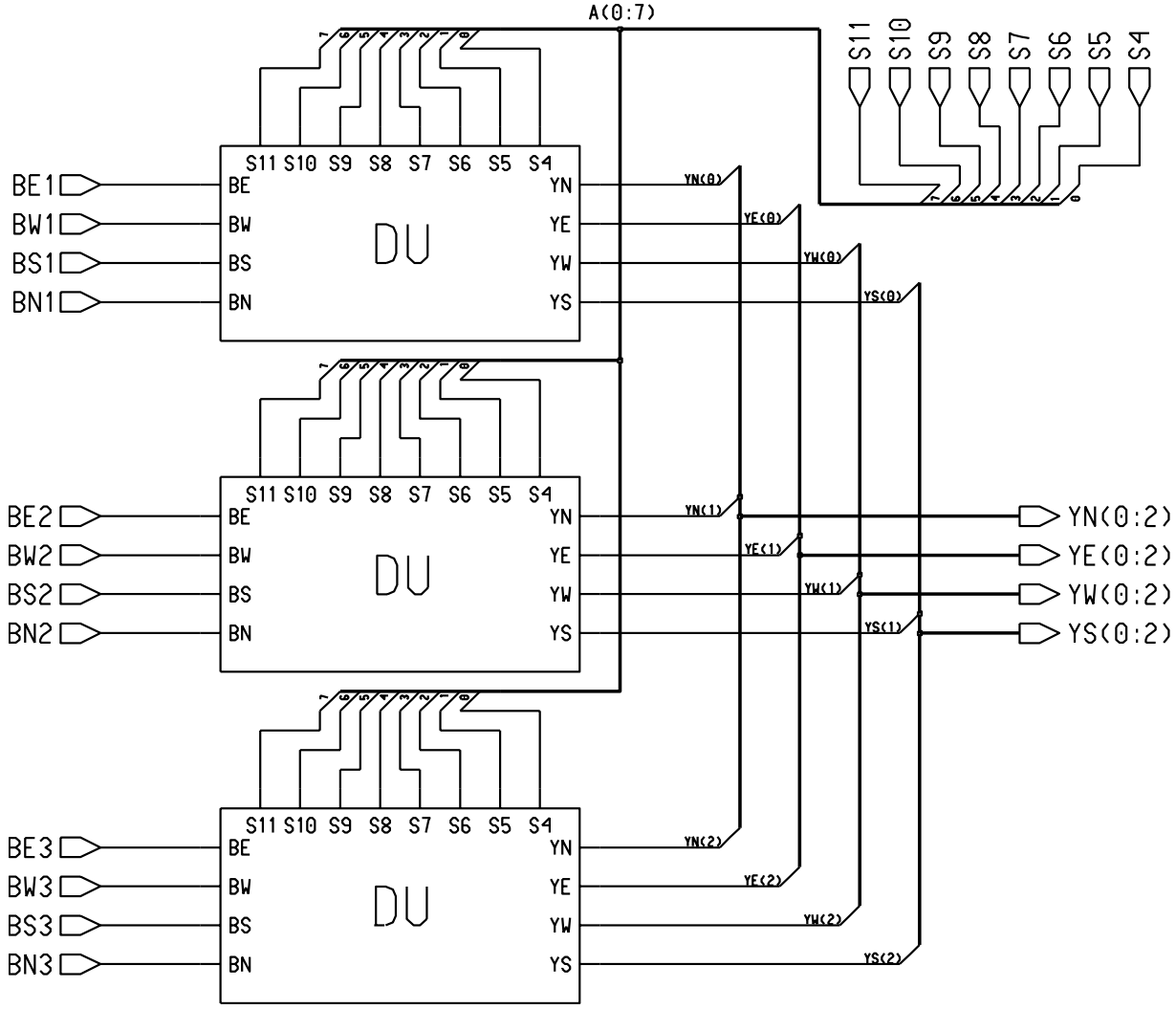
Registered or Combinational Block



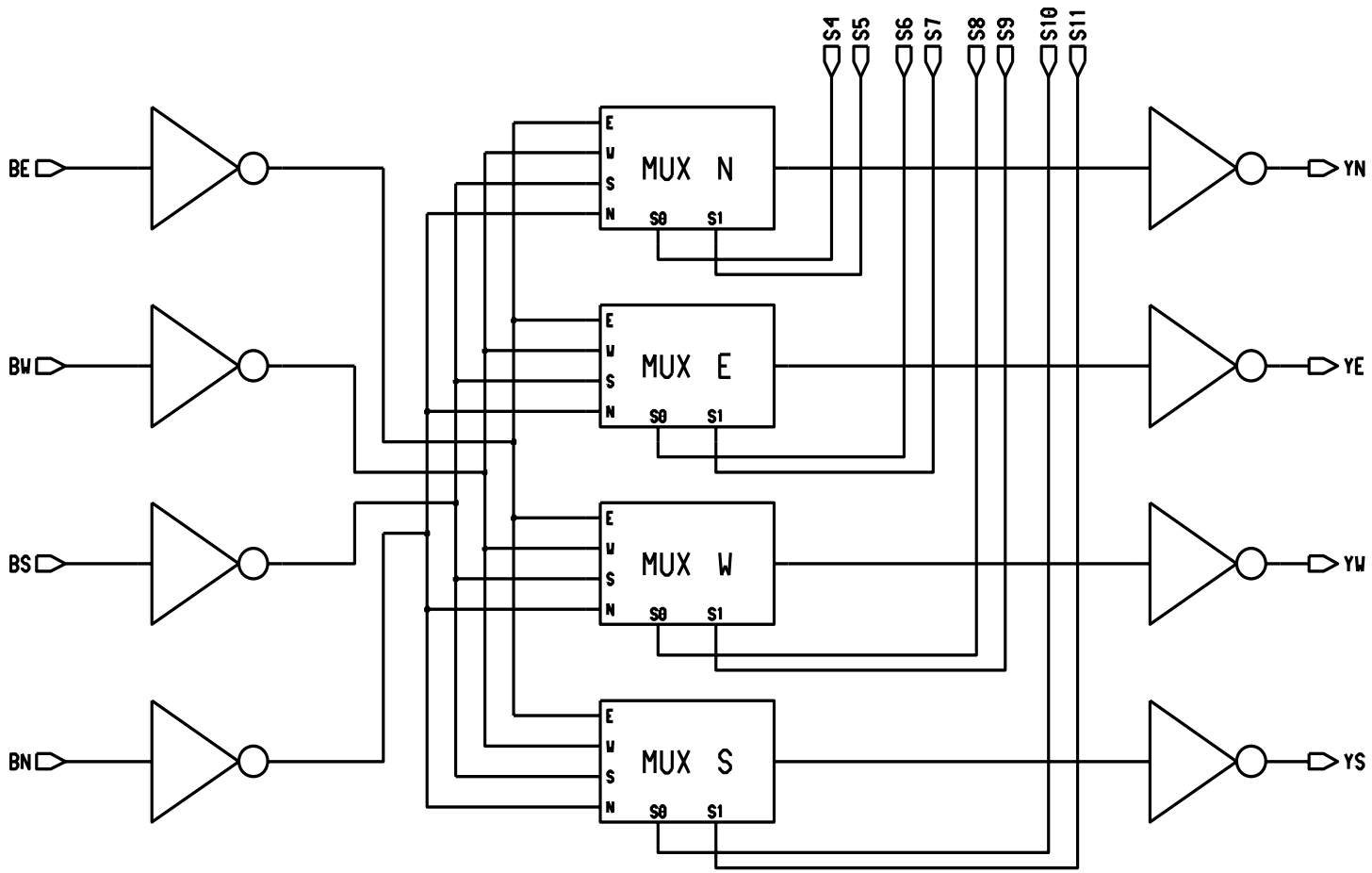
A Logic Block with a Single LUT



Director Block



Director Unit



Configuration Register Bits

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Ctrl Bits	Controls	Description
S_0	MUX 1	Implements feedback loop
S_1	MUX 2	Selects first LUT output or input A_W
S_2	MUX 3	Select A_E or A_W
S_3	ROC	Registered Or Combinational
S_4 S_5	MUX N	Routes any output from Logic Block towards N
S_6 S_7	MUX E	Routes any output from Logic Block towards E
S_8 S_9	MUX W	Routes any output from Logic Block towards W
S_{10} S_{11}	MUX S	Routes any output from Logic Block towards S
S_{12}	MUX 4	Selects second output of the LUT
S_{13}	MUX 5	Select A_S or A_N

Control Register Bit Settings For Various Modes

Modes	S_0	S_1	S_2	S_3	S_4S_5	S_6S_7	S_8S_9	$S_{10}S_{11}$	S_{12}	S_{13}
Registered	*d*	*d*	*d*	1	*dd*	*dd*	*dd*	*dd*	*d*	*d*
Combinational	0	1	*d*	0	*dd*	*dd*	*dd*	*dd*	*d*	*d*
Router	0	0	0	0	*dd*	*dd*	*dd*	*dd*	0	0

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